REMARKS/ARGUMENTS

Status of the Claims

By this paper, Claims 43-74, 83-84, and 89-102 are currently pending, of which Claims 43, 64, and 89 are the pending independent claims. Claims 43, 64, and 89 are amended herein, and Claims 1-42, 75-82, and 85-88 have previously been canceled without prejudice.

Reconsideration and further examination are respectfully requested. No new matter is believed to have been introduced to the application by this paper. The changes to the application are believed to be fully supported by the original disclosure.

Claim Rejections - 35 USC §103

Claims 43, 48-53, 89 and 94-99 are rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,495,442 to Lin et al. (hereinafter "Lin") in view of U.S. Patent No. 6,528,380 to Woolery et al. (hereinafter "Woolery"). Claims 54-59 are rejected under 35 USC 103(a) as being unpatentable over Lin in view of Woolery and U.S. Patent No. 6,235,101 to Erdejac et al. (hereinafter "Erdejac"). Claims 64, 60-63, 69-74, 83, 84 and 100-102 are rejected under 35 USC 103(a) as being unpatentable over Lin in view of Woolery and U.S. Patent No. 6,486,530 to Sasagawa et al. (hereinafter Sagawasa), or over Lin in view of Woolery and Erdejac and Sasagawa. Claims 44-46, 65-67 and 90-92 are rejected under 35 USC 103(a) as being unpatentable over Lin in view of Woolery and Sasagawa, and further in view of U.S. Pub. No. 2003/0155570 to Leidy. Claims 45, 47, 66, 68, 91 and 93 are rejected under 35 USC 103(a) as being unpatentable over Lin in view of Woolery and Sasagawa, and further in view of U.S. Pub. No. 2003/0183332 to Simila.

Claim 43 is directed to a chip structure comprising a silicon substrate, a resistor in the silicon substrate, wherein the resistor comprises silicon with a dopant, a MOS device comprising a portion in the silicon substrate, a metallization structure over the silicon substrate, wherein the metallization structure comprises a first metal layer and a second metal layer over the first metal layer, a first dielectric layer between the first and second metal layers, a passivation layer over the metallization structure and over the first dielectric layer, wherein a first opening in the passivation layer is over a first contact point of a first metal interconnect of the metallization

structure, and the first contact point is at a bottom of the first opening, and wherein a second opening in the passivation layer is over a second contact point of a second metal interconnect of the metallization structure, and the second contact point is at a bottom of the second opening, wherein a gap is between the first and second metal interconnects, wherein the first contact point is connected to the resistor, wherein the passivation layer comprises an insulating nitride layer, and a circuit trace over the passivation layer and on the first and second contact points, wherein the first contact point is connected to the second contact point through the circuit trace.

Claim 89 is directed to a chip structure comprising a silicon substrate, a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant, a MOS device comprising a portion in said silicon substrate, a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer, a dielectric layer between said first and second metal layers, a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein said first contact point is connected to said resistor, wherein said passivation layer comprises an insulating nitride layer, and a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace comprises a copper layer.

For both claims 43 and 89, the Office Action asserts that Lin discloses a chip structure comprising a silicon substrate, a resistor in said silicon substrate (not shown but "transistors and other devices" is described), a MOS device, a metallization structure, a dielectric, a passivation layer, and a circuit trace. The Office Action asserts that Lin fails to disclose the resistor in the silicon substrate and that Woolery teaches a chip structure with a silicon substrate and a resistor in the silicon substrate. The Office Action further asserts that it would have been obvious to one of ordinary skill in the art to modify Lin to have a resistor in the silicon substrate comprising silicon with a dopant as in Woolery. Applicant respectfully disagrees.

The Examiner notes that "*while Lin does not explicitly disclose resistors, the state of the art at the time of the invention provides sufficient evidence to conclude that Lin's disclosure encompasses resistors in the silicon substrate as well.*" (Office Action dated Oct. 30, 2009, pg. 12, lines 7-10) Applicant respectfully traverses the Examiner's opinion. As recited by the Examiner, Lin does not explicitly disclose a resistor in the silicon substrate as claimed in Claims 43 and 89.

Moreover, the applied references are not seen to disclose or suggest at least the features of Claims 43 and 89 of a resistor in the silicon substrate, wherein the resistor comprises silicon with a dopant, a passivation layer over the metallization structure and over the first dielectric layer, wherein a first opening in the passivation layer is over a first contact point of a first metal interconnect of the metallization structure, and the first contact point is at a bottom of the first opening, and wherein a second opening in the passivation layer is over a second contact point of a second metal interconnect of the metallization structure, and the second contact point is at a bottom of the second opening, wherein a gap is between the first and second metal interconnects, wherein the first contact point is connected to the resistor, wherein the passivation layer comprises an insulating nitride layer, and a circuit trace over the passivation layer and on the first and second contact points, wherein the first contact point is connected to the second contact point through the circuit trace.

Accordingly, reconsideration and withdrawal of the rejections of Claims 43 and 89 are respectfully requested.

Claim 64 is directed to a chip structure comprising a silicon substrate, a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant, a MOS device comprising a portion in said silicon substrate, a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer, a dielectric layer between said first and second metal layers, a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein

said first contact point is connected to said resistor, wherein said passivation layer comprises an insulating nitride layer, and a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

The Office Action asserts that Lin discloses a chip structure comprising a silicon substrate, a resistor in said silicon substrate (not shown but "transistors and other devices" is described), a MOS device (not shown but "transistors and other devices" is described), a metallization structure, a dielectric, a passivation layer, and a circuit trace, and also asserts that Lin fails to disclose the resistor in the silicon substrate. The Office Action asserts that Woolery teaches a chip structure with a silicon substrate and a resistor in the silicon substrate and further states that it would have been obvious to one of ordinary skill in the art to modify Lin to have a resistor in the silicon substrate comprising silicon with a dopant as in Woolery. Applicant respectfully disagrees.

The Office Action also asserts that Lin fails to disclose that the circuit trace comprises a titanium-containing layer and a gold layer over the titanium-containing layer. In this regard, the Office Action asserts that Sasagawa teaches a circuit trace comprising a titanium-containing layer and a gold layer over the titanium-containing layer and further states that it would have been obvious to one of ordinary skill in the art to modify Lin to include the different circuit trace and metallization layers of Sasagawa in order to optimize the device performance under thermal stress. Applicant respectfully disagrees.

As stated in the previous argument related to the rejection of claims 43 and 89, Lin does not explicitly disclose resistors. Moreover, the applied references are not seen to disclose or suggest at least the features of Claim 64 of a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant, a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second metal interconnects, wherein said first contact point is connected to said resistor,

wherein said passivation layer comprises an insulating nitride layer, and a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

Furthermore, Lin, Woolery, Erdejac, Sasagawa, Leidy and Simila are not seen to teach, either alone or in combination, the motivation that there could be a circuit with an interconnect with a low resistance accompanying a resistor having an accurate resistance. Applicant teaches that the interconnect is provided over a passivation layer, as currently claimed. The interconnect provided over the passivation layer can be formed with a robust dimension by using a low-cost process due to the underlying metallization structure and MOS devices being protected in advance by a passivation layer. Applicant teaches that the resistor is provided in a silicon substrate, as currently claimed. The resistor provided in the silicon substrate can be formed with accuracy because the resistor can be formed using a precise semiconductor process. The combination of the robust-dimensioned interconnect having low resistance and the accurate resistor can provide an excellent circuit, as claimed by Applicant, which is not disclosed or suggested by Lin, Woolery, Erdejac, Sasagawa, Leidy and Simila.

Accordingly, reconsideration and withdrawal of the rejection of Claim 64 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested. Reconsideration and withdrawal of the rejections of the dependent claims are respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the claims are now in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,
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